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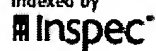
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### 1 [Instantaneous current modeling in a complex VLIW processor core](#)

Radu Muresan, Catherine Gebotys

 May 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 2

Full text available: pdf(3.64 MB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Measuring and modeling instantaneous current consumption or current dynamics of a processor is important in embedded system designs, wireless communications, low-energy mobile computing, security of communications, and reliability. In this paper, we introduce a new instruction-level based macromodeling approach for instantaneous current consumption in a complex processor core along with new instantaneous current measurement techniques at the instruction and program level. Current consumption and ...

**Keywords:** Instruction-level current model, current and power measurement in a processor, instantaneous current model, power and energy model

### 2 [VLSI circuit design: Increasing the energy efficiency of pipelined circuits via slack redistribution](#)

Srivathsan Krishnamohan, Nihar R. Mahapatra

 April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**

Full text available: pdf(178.42 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Technology scaling and rising clock frequencies have made active and leakage power and power density major concerns. Traditional power-reduction techniques, such as dynamic voltage scaling, multi-VDD, gated-VDD, and multi-threshold designs, exploit the slack available in non-critical operations/modes and non-critical areas of the circuit. This limits the amount of power reduction when the circuit is balanced or the critical path dominates the power consumption. We present a systematic technique ...

**Keywords:** low-power design, slack passing, time borrowing

### 3 [Statistics and secret leakage](#)

Jean-Sebastien Coron, David Naccache, Paul Kocher

 August 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 3

Full text available: pdf(218.95 KB)


 Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In addition to its usual complexity assumptions, cryptography silently assumes that information can be physically protected in a single location. As one can easily imagine, real-life devices are not ideal and information may leak through different physical channels. This paper gives a rigorous definition of leakage immunity and presents several leakage detection tests. In these tests, failure *confirms* the probable existence of secret-correlated emanations and indicates how likely the leak is ...

**Keywords:** Cryptography, side-channel analysis

#### 4 Vectorless Analysis of Supply Noise Induced Delay Variation

Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda  
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(289.39 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

The impact of power supply integrity on a design has become a critical issue, not only for functional verification, but also for performance verification. Traditional analysis has typically applied a worstcase voltage drop at all points along a circuit path which leads to a very conservative analysis. We also show that in certain cases, the traditional analysis can be optimistic, since it ignores the possibility of voltage shifts between driver and receiver gates. In this paper, we propose a new analysis ...

#### 5 Built-In Dynamic Current Sensor for Hard-to-Detect Faults in Mixed-Signal ICs

Y. Lechuga, R. Mozuelos, M. Martínez, S. Bracho  
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  pdf(353.98 KB) Additional Information: [full citation](#), [abstract](#), [citations](#)  
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There are some types of faults in analogue and mixed signal circuits which are very difficult to detect using either voltage or current based test methods. However, it is possible to detect these faults if we add to the conventional dynamic power supply current test methods IDDT, the analysis of the changes in the slope of this dynamic power supply current. In this work, we present a Built-In Current Sensor (BICS) which is able to process the highest frequency components in the dynamic power supply current ...

#### → 6 On the interaction of power distribution network with substrate


Rajendran Panda, Savithri Sundareswaran, David Blaauw  
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available:  pdf(150.54 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

**Keywords:** power grid analysis, substrate analysis, substrate coupled noise, substrate noise

#### → 7 JouleTrack: a web based tool for software energy profiling

Amit Sinha, Anantha P. Chandrakasan  
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available:  pdf(209.31 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


A software energy estimation methodology is presented that avoids explicit characterization of instruction energy consumption and predicts energy consumption to within 3% accuracy

for a set of bench-mark programs evaluated on the StrongARM SA-1100 and Hitachi SH-4 microprocessors. The tool, JouleTrack, is available as an online resource and has various estimation levels. It also isolates the switch-ing and leakage components of the energy consumption.

**Keywords:** instruction energy, leakage estimation, software energy

→ 8 High-level simulation of substrate noise generation including power supply noise coupling

Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens  
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available:  pdf(114.20 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Substrate noise caused by large digital circuits will degrade the performance of analog circuits located on the same substrate. To simulate this performance degradation, the total amount of generated substrate noise must be known. Simulating substrate noise generated by large digital circuits is however not feasible with existing circuit simulators and detailed substrate models due to the long simulation times and high memory requirements. We have developed a methodology to simulate this su ...

→ 9 Energy estimation for 32-bit microprocessors

C. Brandolese, W. Fornaciari, F. Salice, D. Sciuto  
May 2000 **Proceedings of the eighth international workshop on Hardware/software codesign**

Full text available:  pdf(221.39 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Estimation of software power consumption is becoming one of the major problems for many embedded applications. The paper presents a novel approach to compute the energy of an Instruction Set, through a suitable functional decomposition of the activities involved during instruction execution. One of the main advantages of this approach is the capability to predict the power figures of the overall Instruction-Set starting from a small subset. A formal discussion on the statis ...

→ 10 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli  
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2



Full text available:  pdf(385.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)




This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

→ 11 A digital partial built-in self-test structure for a high performance automatic gain control circuit

A. Lechner, J. Ferguson, A. Richardson, B. Hermes  
January 1999 **Proceedings of the conference on Design, automation and test in Europe**



Full text available:  pdf(117.14 KB) Additional Information: [full citation](#), [citations](#), [index terms](#)

- 12 Full-chip verification of UDSM designs   
 R. Saleh, D. Overhauser, S. Taylor  
 November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**  
 Full text available:  pdf(879.89 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

- 13 Full-chip verification methods for DSM power distribution systems   
 Gregory Steele, David Overhauser, Steffen Rochel, Syed Zakir Hussain  
 May 1998 **Proceedings of the 35th annual conference on Design automation**  
 Full text available:  pdf(543.14 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)  
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Power distribution verification is rapidly becoming a necessary step in deep submicron (DSM) design of high performance integrated circuits. With the increased load and reduced tolerances of DSM circuits, more failures are being seen due to poorly designed power distribution systems. This paper describes an efficient approach for the verification of power distribution at the full-chip transistor level based on a combination of hierarchical static and dynamic techniques. Application of the m ...

**Keywords:** IR-drop, PowerPC, power distribution network, reliability

- 14 Signal processing at 250 MHz using high-performance FPGA's   
 Brian Von Herzen  
 February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**  
 Full text available:  pdf(1.06 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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